ABSTRACT OF THE DISCLOSURE

The present invention provides a large scale integrated circuit which is capable of coping with the problems associated with the situation in which the number of pins used in the circuit is increased, and is capable, even when dummy bumps (DBPs) are installed, of suppressing storage of an excessive charge to the DBPs and prevent discharge to adjacent bump electrodes and prevent breakdown of a semiconductor chip due to electrostatic noise. On the element formation face of the semiconductor chip where pads (PDs) are formed, a layer insulating film for rewiring, external bumps (EBPs) that correspond respectively to PDs formed on the layer insulating film, dummy bumps (DBPs) lacking corresponding PDs on the semiconductor chip, external bump rewirings that connect the PDs and the corresponding EBPs, and dummy bump rewirings that connect DBPs and prescribed EBPs are formed in addition. An electrostatic protection means is installed between a PD connected to an EBP that is connected to a DBP and an internal circuit section or an I/O circuit section of the semiconductor chip.